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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,965	01/16/2002	Shiann Liou	MP0116	1558

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MARVELL SEMICONDUCTOR, INC.
INTELLECTUAL PROPERTY DEPARTMENT
700 FIRST AVENUE, MS# 509
SUNNYVALE, CA 94089

EXAMINER

THAI, LUAN C

ART UNIT PAPER NUMBER

2827

DATE MAILED: 12/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/051,965

Applicant(s)

LIOU, SHIANN

Examiner

Luan Thai

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10/9/02
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 January 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2&5.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of group I, claims **1-16** in Paper No. 8 filed October 09, 2002 is acknowledged.

Claims 1-16 are pending in this application.

Claims 17-24 have been canceled.

Information Disclosure Statement

2. The information disclosure statements (IDS) filed on 01/16/02 and 5/13/02 have been considered by the examiner.

Oath/Declaration

3. The declaration filed 01/16/02 is acceptable.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-2, 6-10, and 14-16, are rejected under 35 U.S.C. 102(b) as being anticipated by Fjelstad (5,989,939).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1-2, 6-10, and 14-16, Fjelstad disclose (see specifically figures 13-14) an integrated circuit comprising: a semiconductor die 21 including

a plurality of pairs of bond pads 23/24 (or electrical termination means), each pair of bond pads 23/24 (or electrical termination means) having a single corresponding bond wire 25 (or means for conducting) connected thereto such that each bond pad (or electrical termination means) of each of the pairs of bond pads (or pair of electrical termination means) has only one bond wire end (or only one end of any means) connected thereto, a first bond pad 24 (or first electrical termination means) of each pairs of bond pads (or each pair of electrical termination means) located in an internal portion of the semiconductor die, and a second bond pad 23 (or second electrical termination means) of each pairs of bond pads (or each pair of electrical termination means) located along a periphery and in the internal portion of the semiconductor die 21, wherein the bond wire is a signal interconnects (Col. 9, lines 8+).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 3-5 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fjelstad (5,989,939) in view of Manning et al. (6,169,331 applicant admitted prior art).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 3-4 and 11-12, Fjelstad discloses all the limitations of the claimed invention as detailed above except for specifying the material (e.g., either gold, aluminum, or copper) of the bond wire (or means for conducting).

Gold and aluminum, however, are well-known materials in semiconductor art for making bond wires, as taught by Manning et al. (Col. 4, lines 11+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use gold or aluminum bond wire in Fjelstad 's integrated circuit since such materials are known and conventionally used in art for making bond wire, as disclosed by Manning et al.

Regarding claims 5 and 13, Fjelstad discloses all the limitations of the claimed invention as detailed above except for a trace connected between the pair of bond pads (or pair of electrical termination means).

Manning et al. while related to a similar integrated circuit die design teach (see specifically figure 3A) a pair of bond pads 121a-121b are connected together not only by bond wire 150b (outside the semiconductor die 120) but also by the trace 153 (inside the semiconductor die 120) in order to reduce electrical resistance between the two bond pads 121a-121b (Col. 4, lines 59+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Fjelstad's integrated circuit by forming an additional trace in the semiconductor die 21 connected between the pair of bond pads 23/24, as taught by Manning et al., in order to reduce electrical resistance between the two bond

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pads, and such modification is held to be within the ordinary designing ability expected of a person skilled in the art.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is (703) 308-1211. The examiner can normally be reached on 7:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A handwritten signature in black ink, appearing to read 'Luan Thai', with a long, sweeping horizontal line extending to the right.

Luan Thai
December 12, 2002